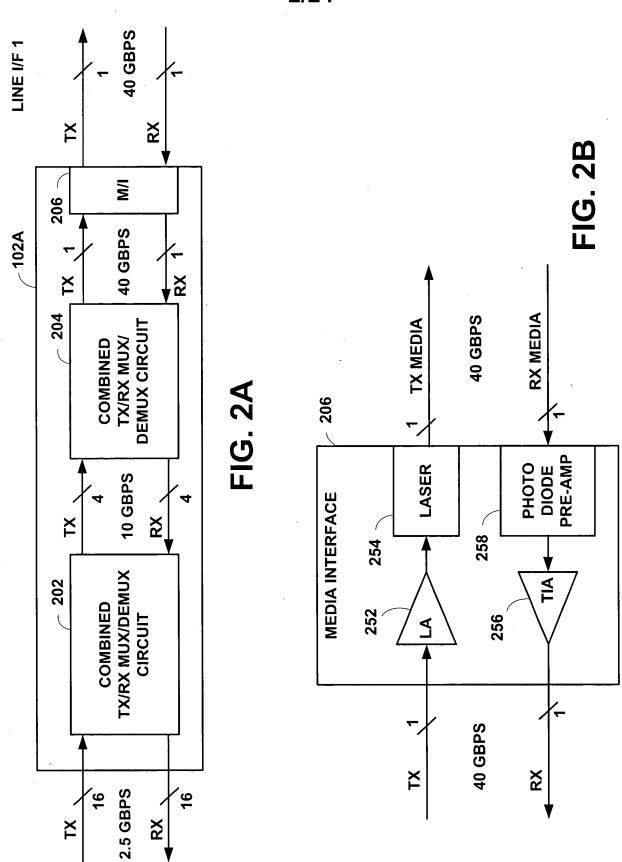


FIG. 1



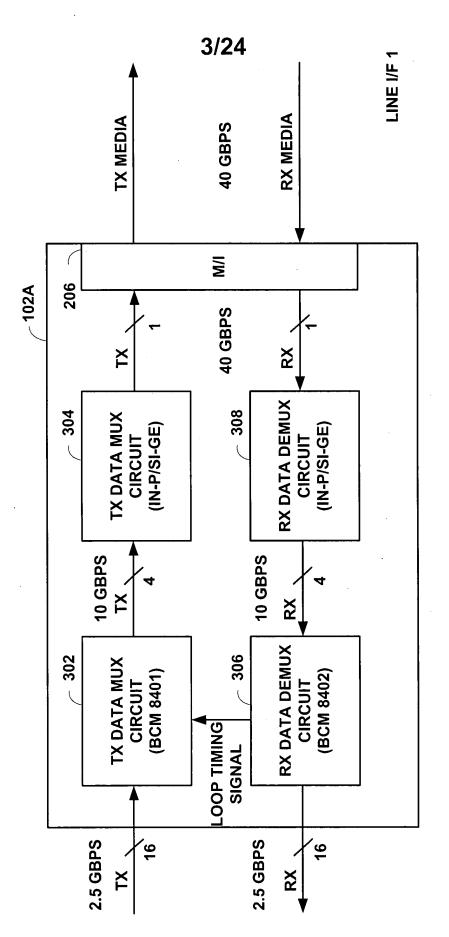
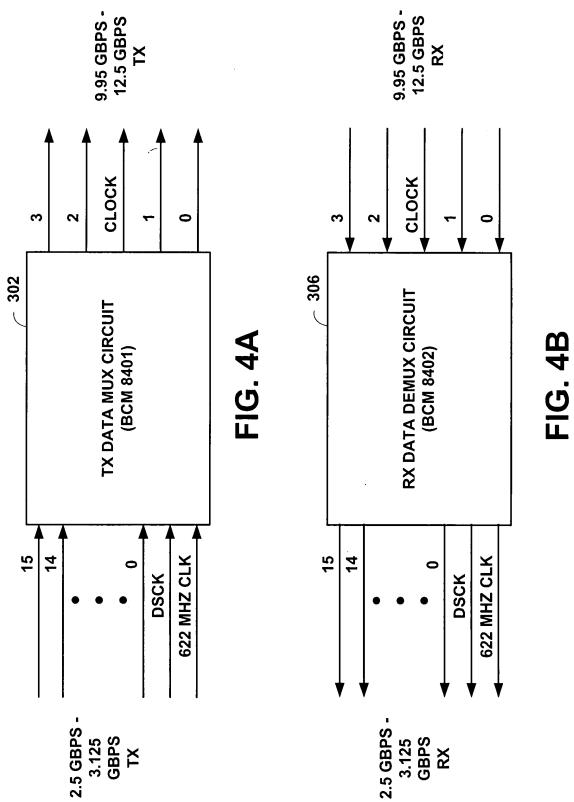
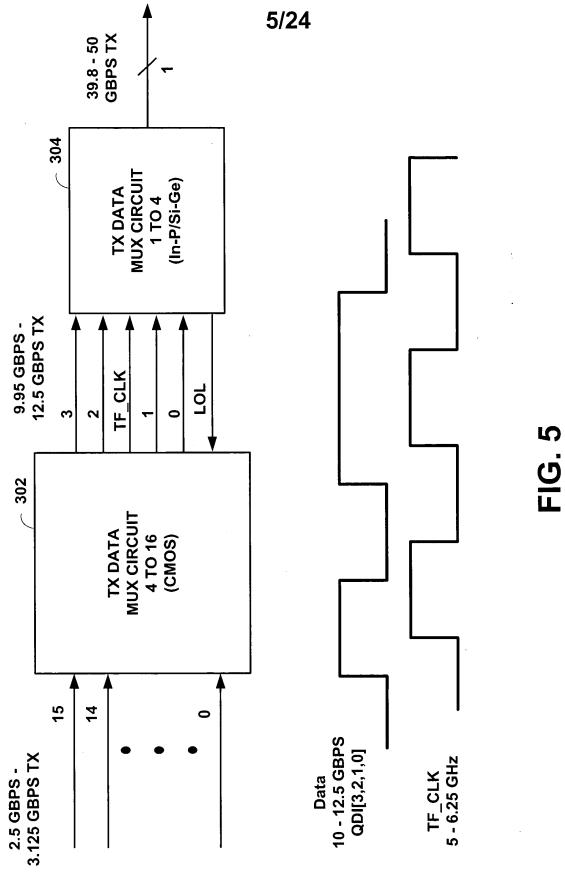


FIG. 3





Receiver Input and Source Centered Clock Performance	lock Perfo	rmance				
Parameter	Symbol	Conditions	Min	Typ	Max	Units
Output Common Mode	Vcm	See Figure Below	1575	1675	1775	mV
Single Ended Output Impedance	Z_{SE}		40	20	09	C
Differential Input impedance	Z_{d}		80	100	120	G
Input Impedance Mismatch	$Z_{\scriptscriptstyle M}$				10	%
Q40, CML Input Differential Amplitude, p-p	A VQDO	See Figure Below	400	200	009	mV
Q40 Input Rise and Fall Time (20% to 80%)	t _{rH} , t _{FH}			25	35	šd
Differential output return loss*	S11	Up to 7.5 GHz	10			фВ
4-by-1 mux input return loss >15 db at 10 GHz] '			
	:					400
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	8.1 \$600 \$8.1 \$600 \$8.1 \$8.1 \$8.1 \$8.1 \$8.1 \$8.1 \$8.1 \$8.1	Q40 Receive r A040 Receive r r		405 F	FIG. 6	!

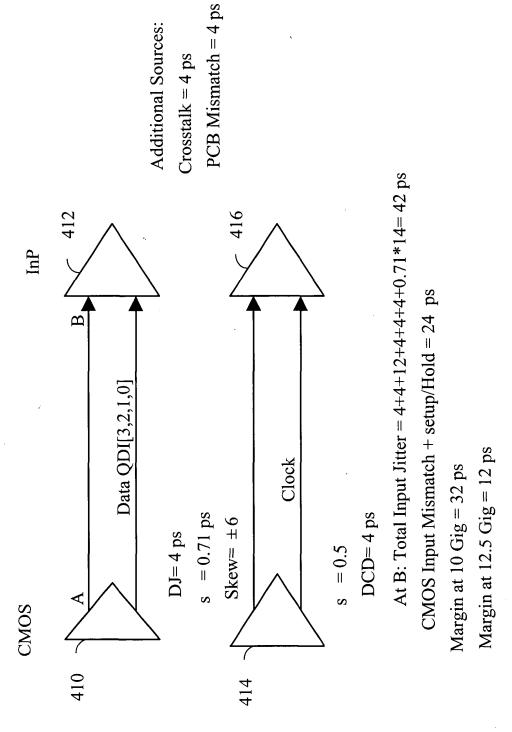
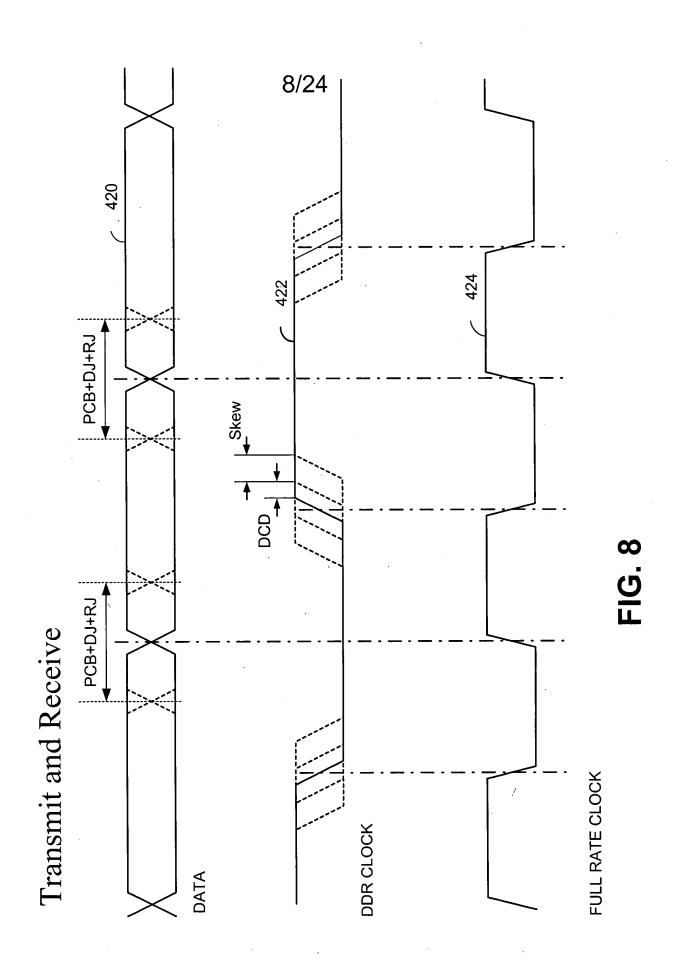
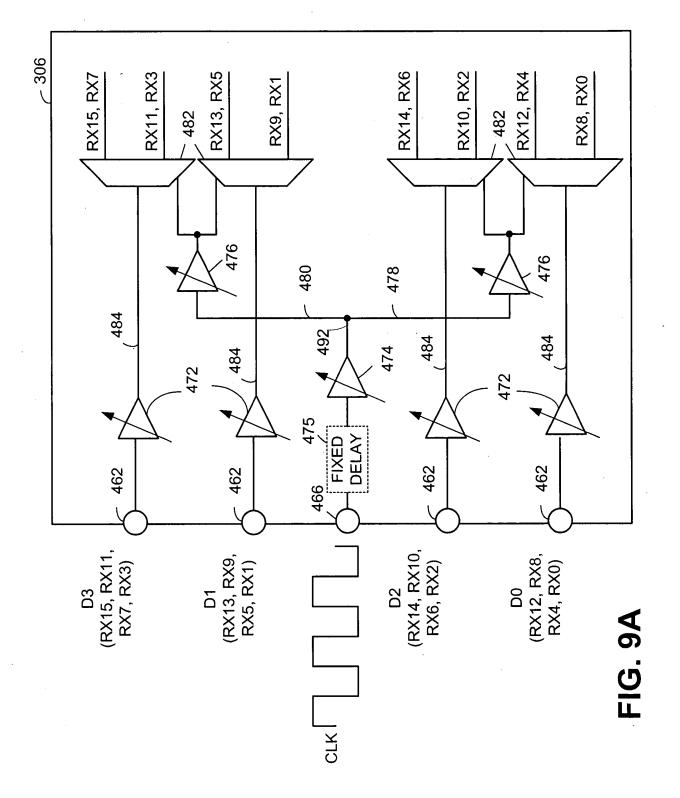


FIG. 7





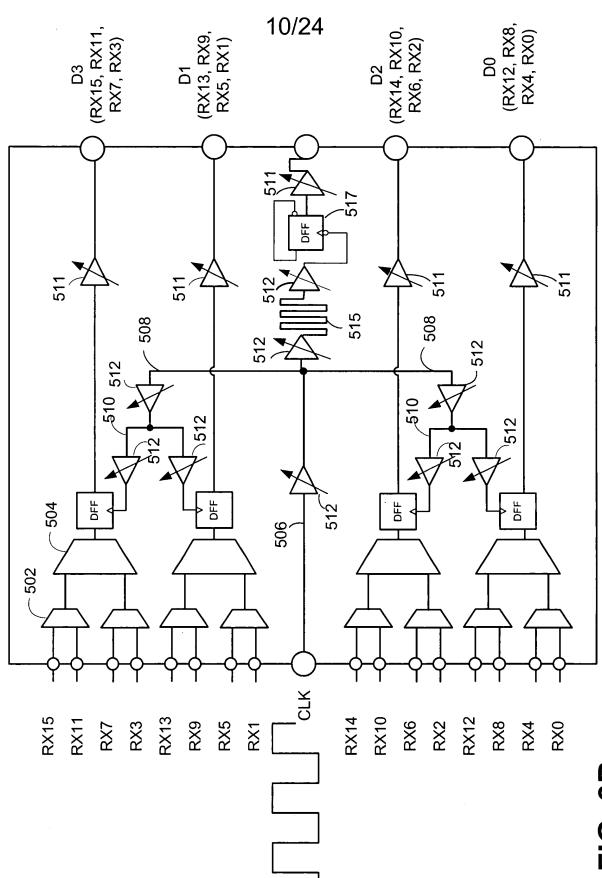


FIG. 9B

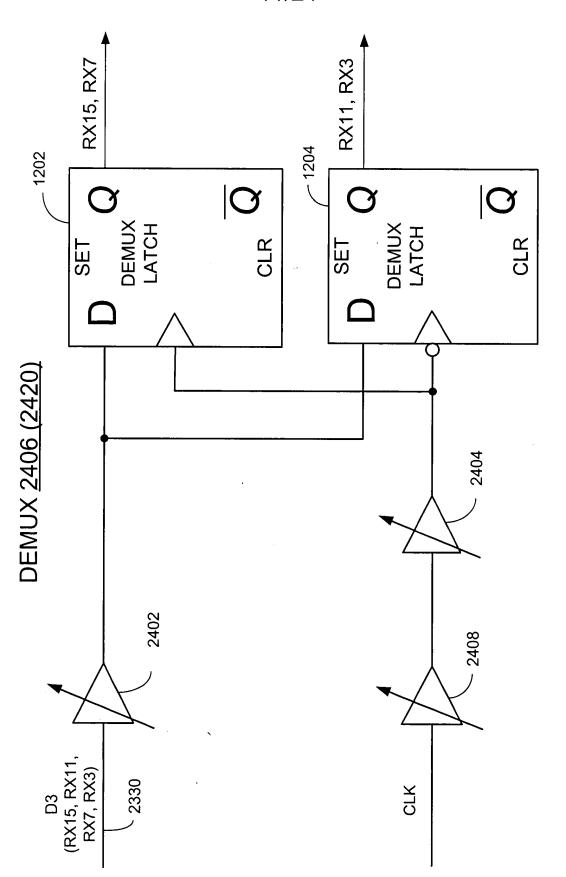


FIG. 10A

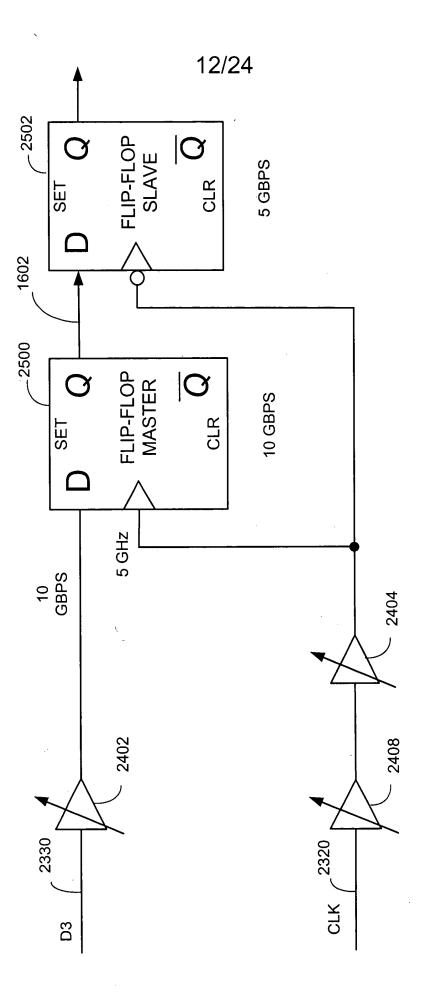
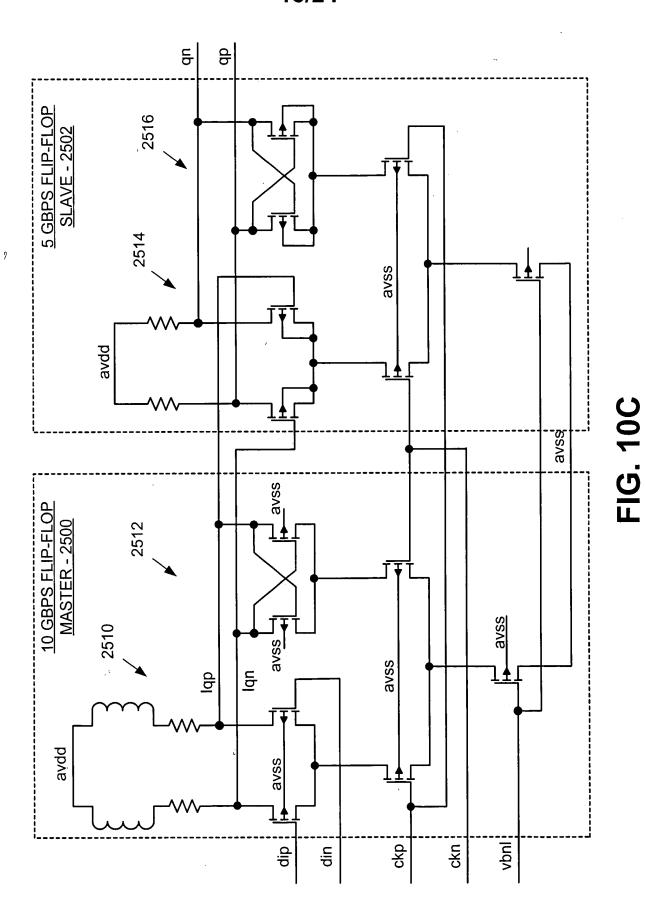


FIG. 10B



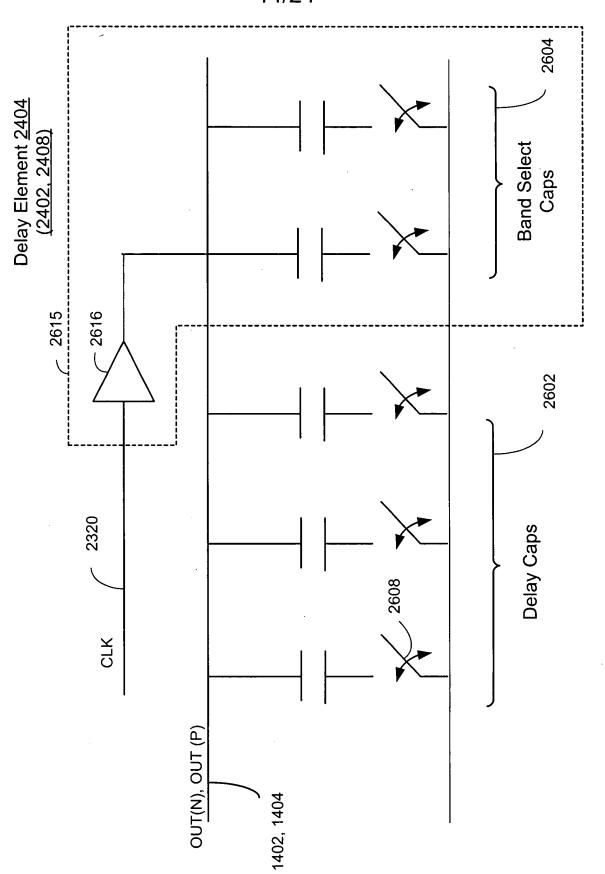
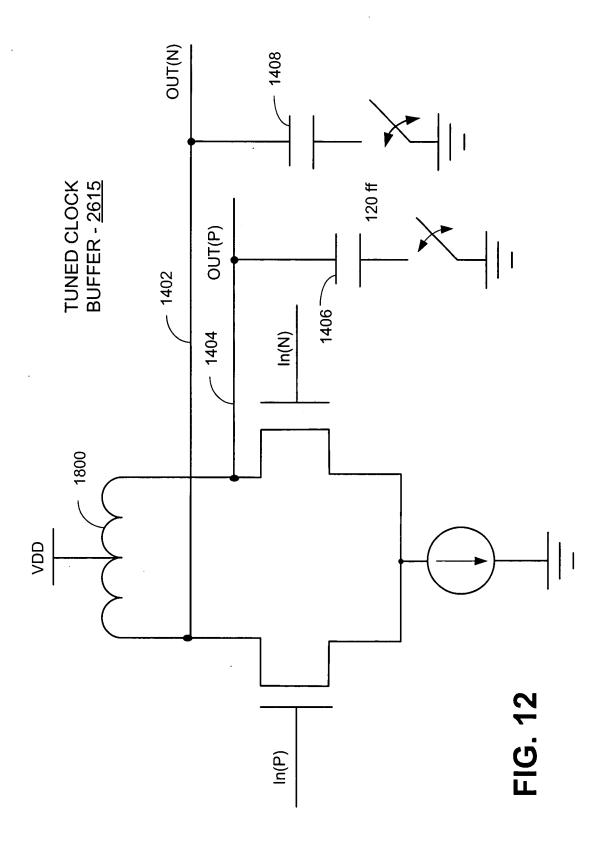


FIG. 11



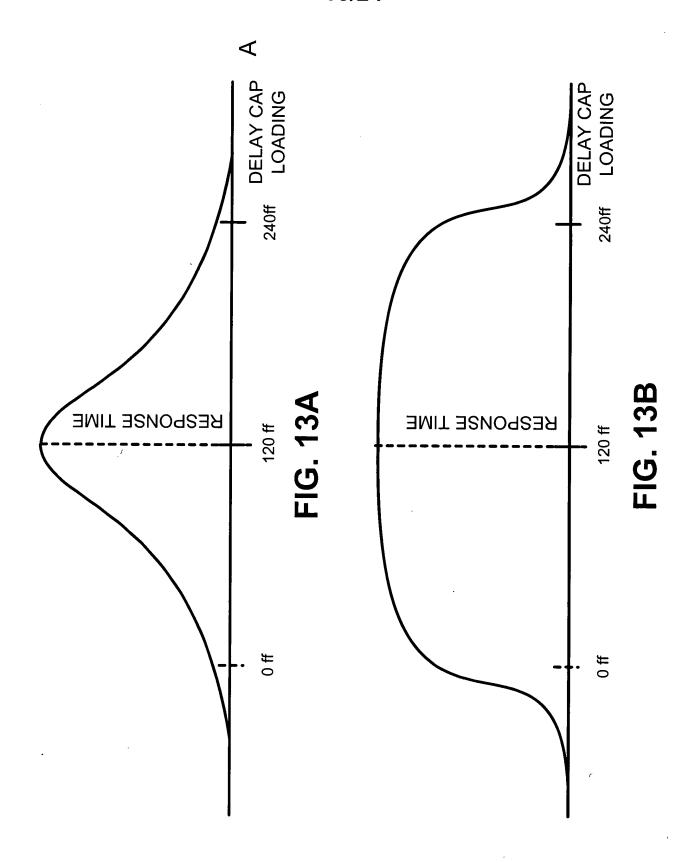


FIG. 14A

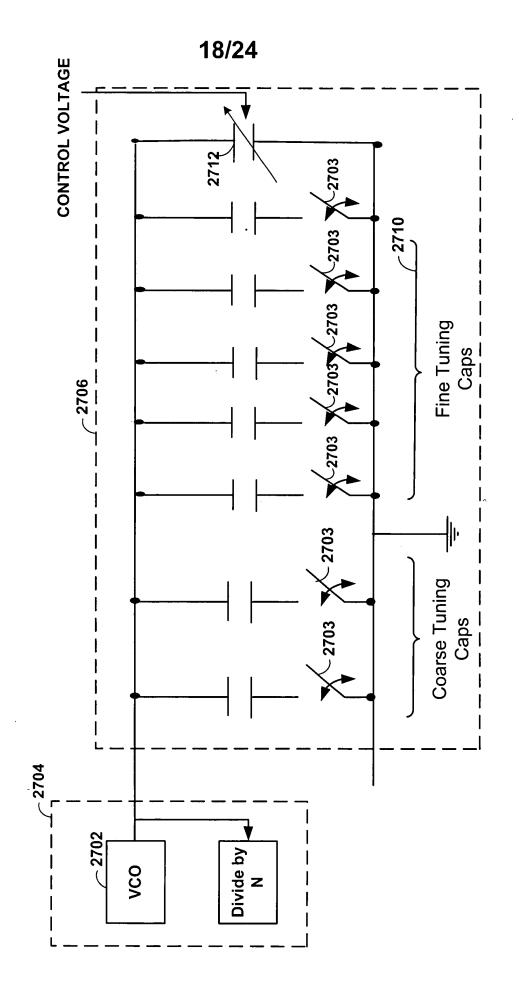
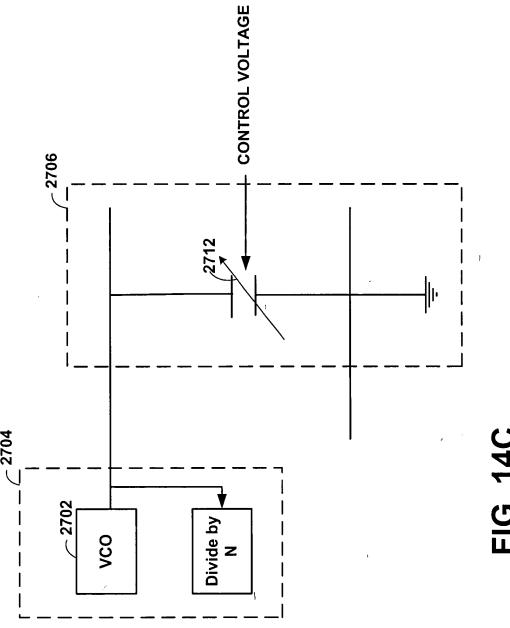


FIG. 14B



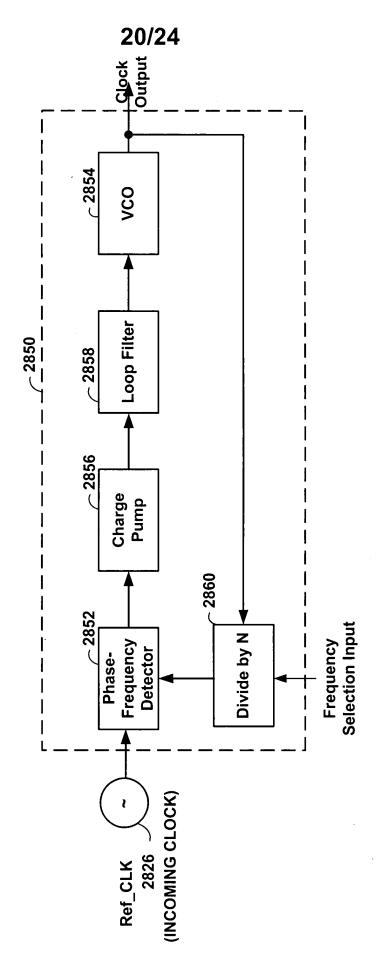
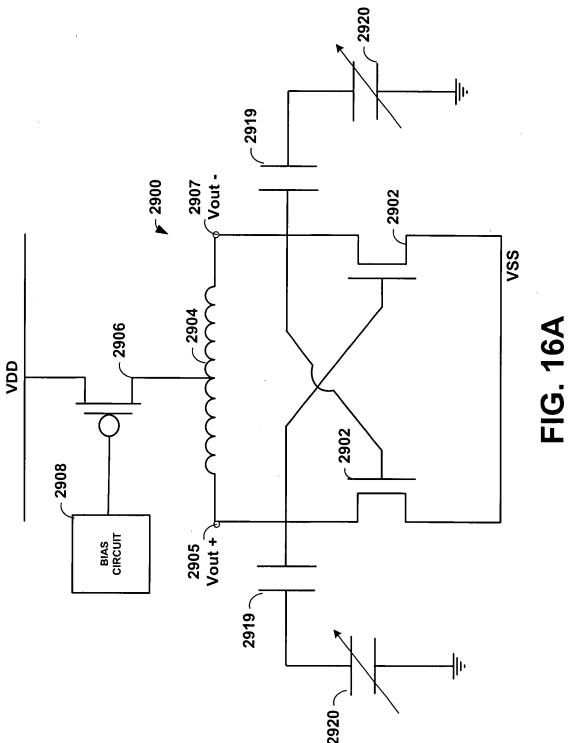
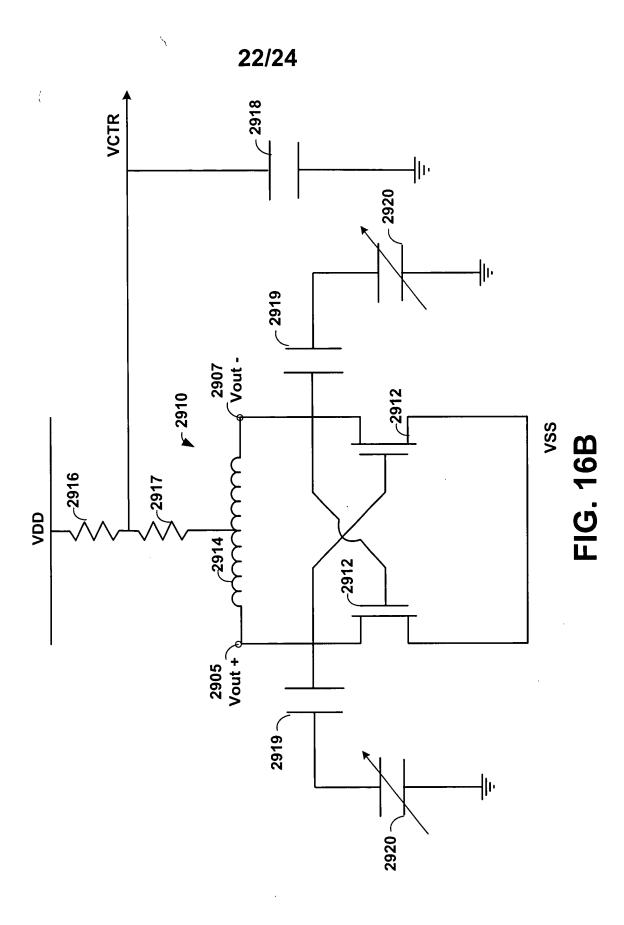


FIG. 15





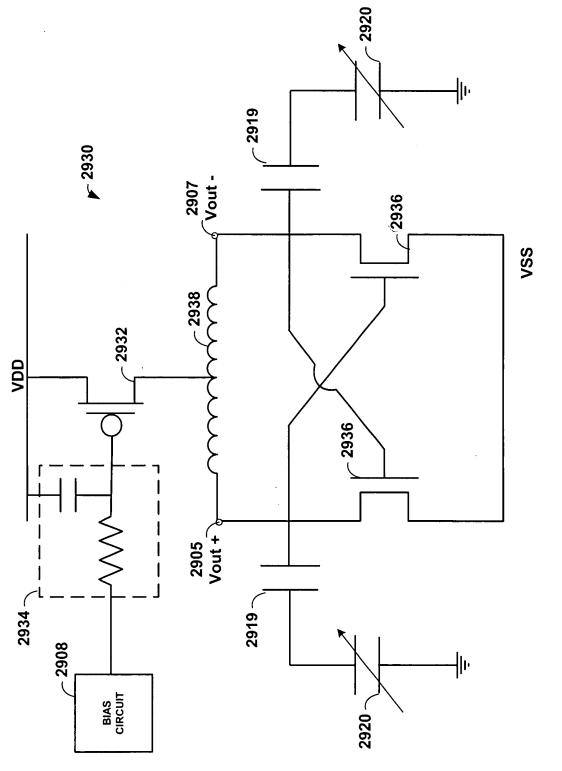


FIG. 16C



